Co-funded by the Horizon 2020
Framework Programme of the European Union

Fabrication and assembly automation of **Ter**abit optical transceivers based on **I**nP EML arrays and a **P**olymer **h**ost platform for optical **i**nter**c**onnects up to 2 km and beyond

Call identifier:

H2020-ICT-4-2018

Contract No:

825502

Partners:

- Inst. Of Comm. And Computer Systems/ National Tech. University of Athens (ICCS/NTUA) – GR (coordinator)
- Fraunhofer Heinrich Hertz Institute (FhG-HHI) – GE
- ficonTEC (FIC) – GE
- III-V Lab (III-V Lab)– FR
- Mellanox Technologies (MLNX) – IL
- Telecom Italia SPA (TIM) – IT

Timeline:

January 2019 – December 2021

Budget:

Overall budget: € 5 626 642,50

EC contribution: € 4 737 468,75

Contact:

Prof. Hercules Avramopoulos

Dr. Panos Groumas

Photonics Commun. Research Laboratory

National Technical University of Athens

Tel: +30 210 772 2057

Project website:
www.ict-teriphic.eu

Motivation

The capability to provide Terabit capacity and the possibility for high-volume production at low cost are the two main requirements that rule today the development of next generation optical modules for datacom applications. The current 400G Ethernet standards were approved only a few months ago, but the efforts to develop the next optical modules providing Terabit capacity have already kicked off. A practical path to the Terabit regime is to scale the current 400G modules, which are based (in the most forward looking version of the standards) on 4 parallel lanes, each operating with PAM-4 at 53 Gbaud. Scaling these modules by adding lanes looks simple, but entails challenges with respect to the fabrication and assembly complexity that can critically affect their manufacturability and cost. This is particularly the case, when the optical modules are based on micro-optics solutions for the integration of the individual components and their final assembly and packaging. Photonic integrated circuit (PIC) technology on the other hand can offer alternative solutions and can become the key enabler for the addition of lanes and the extension of capacity to the Terabit regime, but only when the integration and assembly concepts are kept simple and reliable.

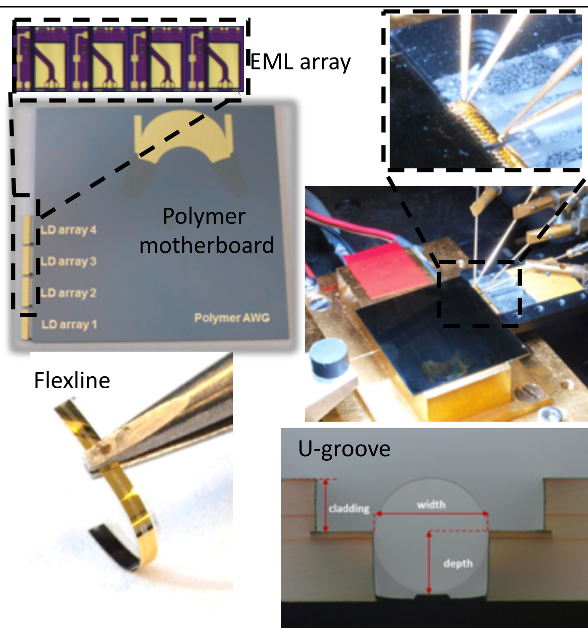

Figure 2: Photographs of the TERIPHIC toolbox (polymer host motherboard, the EML array, the flexline, the U-groove) and the alignment process that will be automatized.

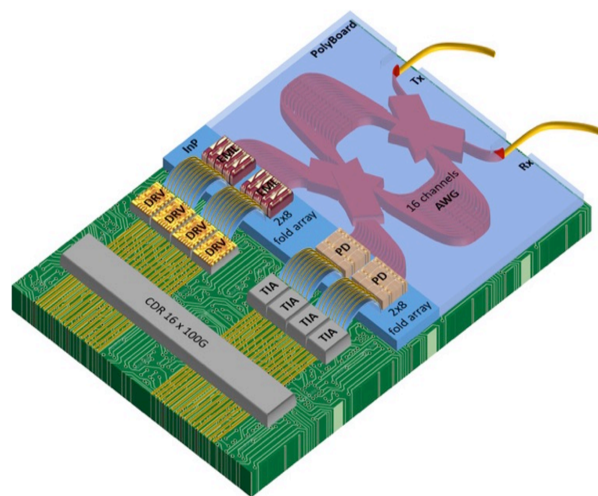

Figure 1: **Artistic layout of TERIPHIC 1.6 Tb/s transceiver module capable of operation at 100G per lane utilizing 53Gbaud PAM-4.**

TERIPHIC in a pragmatic innovation action that aims to address these challenges by leveraging photonic integration concepts and developing a seamless chain of component fabrication, assembly automation and module characterization processes as the basis for high-volume production lines of Terabit modules.

Concept and objectives

TERIPHIC will bring together EML arrays in the O-band, PD arrays and a polymer chip that will act as the host platform for the integration of the arrays and the wavelength mux-demux of the lanes. The integration will rely on butt-end-coupling steps, which will be automated via the development of module specific alignment and attachment processes on commercial equipment. The optical subassembly will be mounted on the mainboard of the module together with linear driver and TIA arrays. The assembly process will be based on the standard methodologies of MLNX and the use of polymer FlexLines for the interconnection of the optical subassembly with the drivers and the TIAs. Using these methods, TERIPHIC will develop pluggable modules with 8 lanes (800G capacity) and mid-board modules with 16 lanes (1.6T capacity) having a reach of at least 2 km. Compared to the 400G standards, the modules will reduce by 50% the power consumption per Gb/s, and will have a cost of 0.3 Euro/Gb/s. After assembly, the modules will be mounted on the line cards of MLNX switches, and will be tested in real settings. A study for the consolidation of the methods to make them suitable for very high-volume production will be also made.

Exploitation and expected impact

TERIPHIC aims to industrialize the foreground that will be generated within the project and establish viable exploitation paths in order to reinforce the European industrial competeti-veness. The envisioned exploitation strategy involves the manufacturing level and the module level:

At the manufacturing level, TERIPHIC will prepare a clear roadmap towards the set up of a pilot assembly line in the post-project era, supported by the projec. It will also aim to standardize the optimized key processes and the automated assembly steps.

At the module level, TERIPHIC will employ Mellanox as the main exploitation route for the transceivers. Mellanox as a leading supplier in Ethernet DC equipment, will incorporate the TERIPHIC modules to its product line.