TERIPHIC

Fabrication and assembly automation of TERabit optical transceivers based on InP EML arrays and a Polymer Host platform for optical InterConnects up to 2 km and beyond

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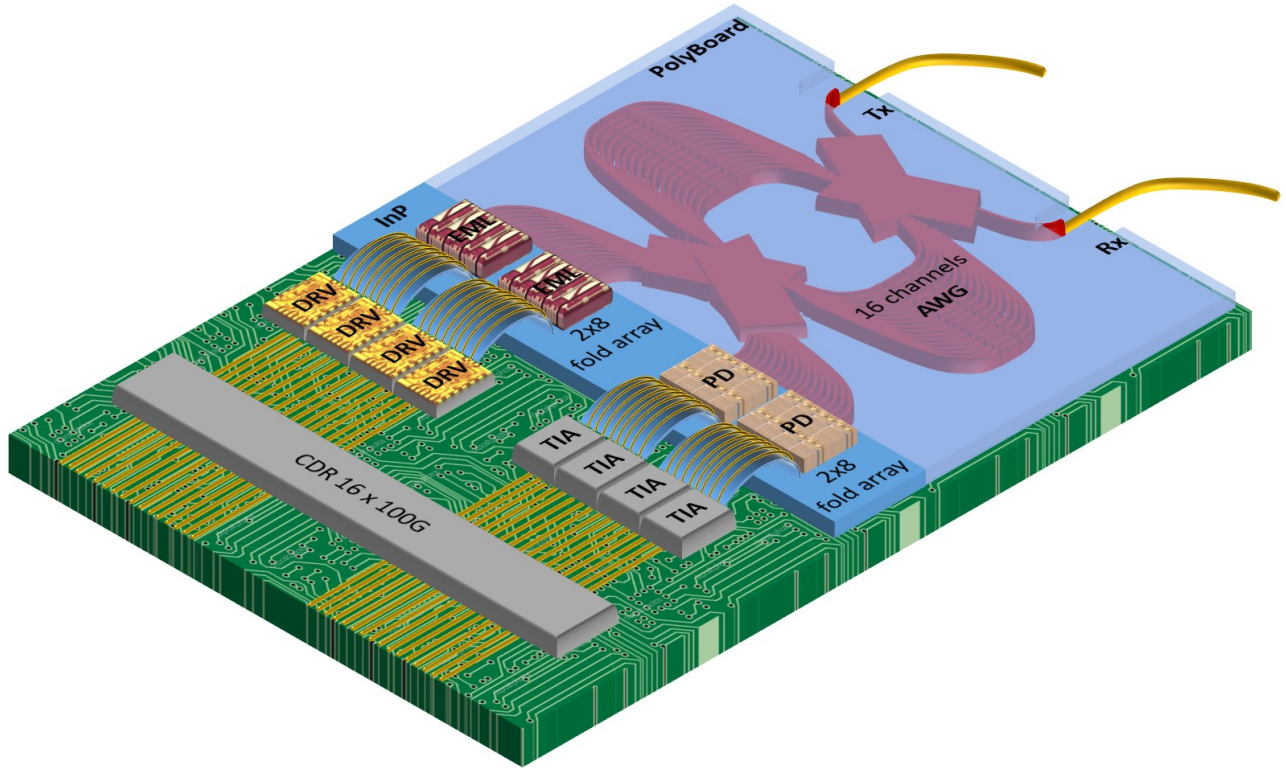
Type of action: Innovation Action (IA)

Project start: Jan 1, 2019

Duration: 3 years

Overall budget: € 5 626 642,50

EC contribution: € 4 737 468,75



Co-funded by the Horizon 2020
Framework Programme of
the European Union

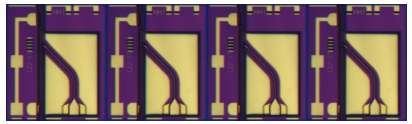
Consortium

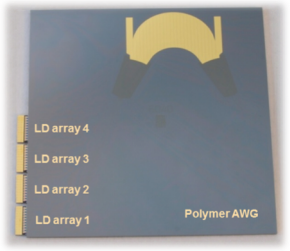
- Institute of Communications and Computer Systems/ National Technical University of Athens – ICCS/NTUA (GR)
- Fraunhofer Gesellschaft Heinrich Hertz Institute – FhG-HHI (GE)
- FiconTEC – FIC (GE)
- III-V Lab – III-V Lab (FR)
- Mellanox Technologies Ltd – MLNX (IL)
- Telecom Italia SPA – TIM (IT)

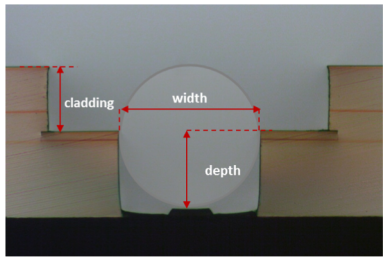
Motivation

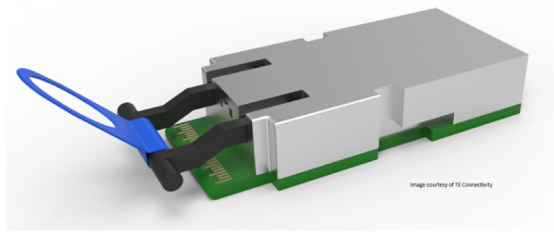
A practical path to the Terabit regime is to scale the current 400G modules, which are based (in the most forward looking version of the standards) on 4 parallel lanes, each operating with PAM-4 at 53 Gbaud. Scaling these modules by adding lanes looks simple, but entails challenges with respect to the fabrication and assembly complexity that can critically affect their manufacturability and cost.

TERIPHIC aims to address these challenges by leveraging photonic integration concepts and developing a seamless chain of component fabrication, assembly automation and module characterization processes as the basis for high-volume production lines of Terabit modules









Approach (I)

1. Simplify transceivers' photonic part and eliminate time consuming processes

    a) Rely on multi-functional optoelectronic components

    b) Use PolyBoard as host platform for TOSA/ROSA development

2. Develop arrayed versions of components to increase capacity in a single optical subassembly w/o increasing integration steps

3. Develop an automated, high-throughput and reliable assembly process for TOSAs/ROSAs

4. Rely on high-speed electronic and optoelectronic components to achieve 100 Gb/s per lane

Approach (II)

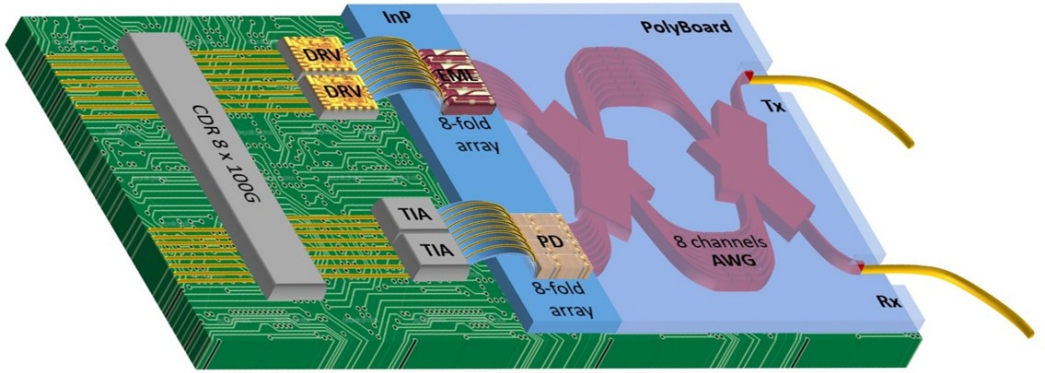
5. Use automated assembly process to fabricate pluggable and mid-board transceivers with Terabit capacity

6. Lower transceiver cost to <1 € per Gb/s

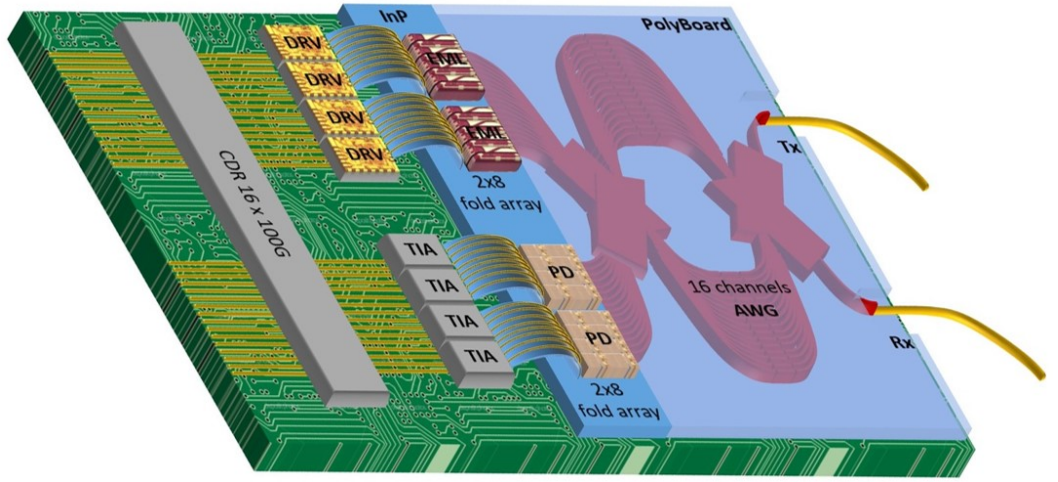
7. Validate TERIPHIC transceivers in intra- Data Center Networks up to 2 km

8. Explore TERIPHIC transceivers for inter- DCNs beyond 2 km

Module 3 – Pluggable 800 Gb/sec total capacity – 50 Gbaud PAM-4



Module 4 – Mid board 1600 Gb/sec total capacity – 50 Gbaud PAM-4



Objectives (I)

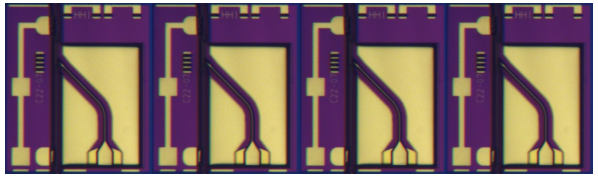
1. Develop EML arrays, PD arrays and Polymer motherboards

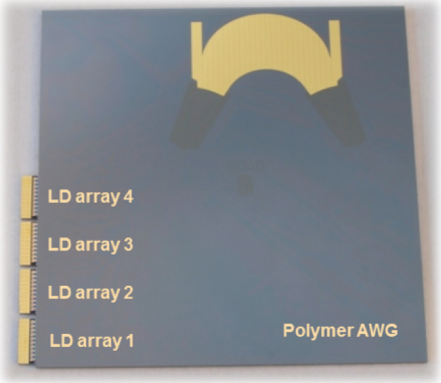
O-band operation

8-fold EML arrays with >50 GHz bandwidth

8-fold PD arrays with > 50 GHz bandwidth

16-ch AWG MUX-DEMUX on PolyBoard (<5 dB loss)





PolyBoard will host the EMLs, PDs, and fiber pigtails.

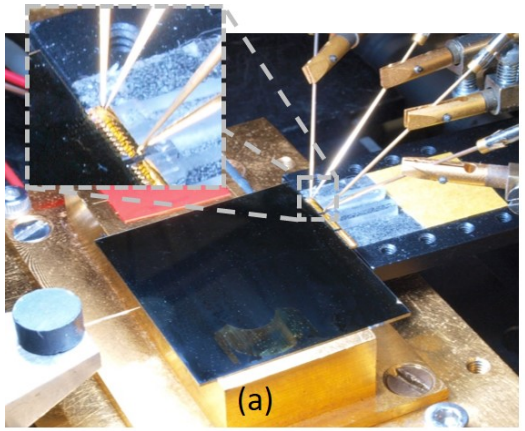
2. Develop automated assembly process for the optical assembly of the Tb/s transceivers

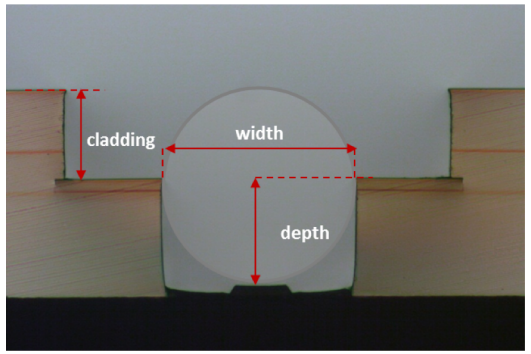
Automate passive and active alignment of EML array chips and PD array chips to PolyBoard

Automate fiber pigtail gripping and attachment to PolyBoard

Automate UV resin dispensing and curing

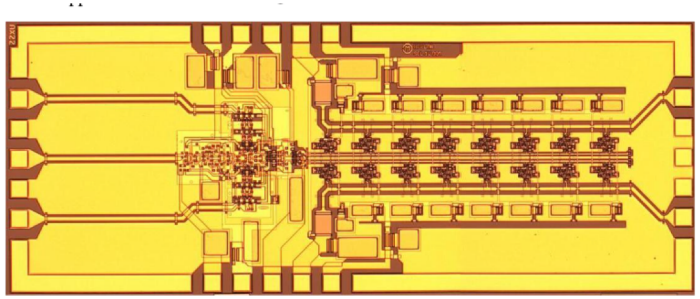
Automate placement of PolyBoard on carrier chip





Objectives (II)

3. Fabricate high-speed linear driver arrays and TIA arrays



Develop quad linear driver arrays on InP-DHBT platform. Optimize output voltage and power consumption

Select high bandwidth > 35 GHz linear drivers with high output amplitude. Select high bandwidth TIA circuits with appropriate gain and output ampl. Select appropriate supporting circuits e.g. gearboxes, CDRs

4. Develop automated assembly and packaging engine leveraging the polymer Flexlines

Develop high bandwidth Polymer FlexLines as flexible tapes

Connect many driver/TIA interfaces and the optical subassembly in a single assembly step

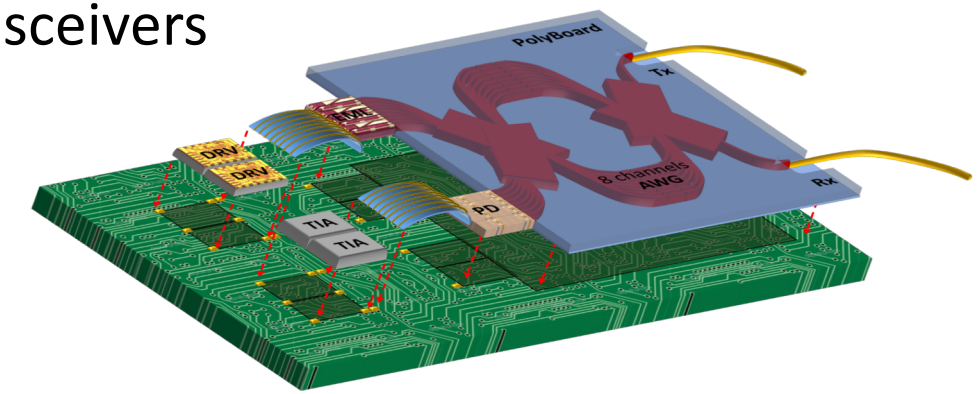
Objectives (III)

5. Develop small form factor pluggable and mid-board transceivers

Develop transceiver mainboards for 50 Gbaud operation

Select supporting electronic circuits

Integrate TOSA/ROSA chip-on-carrier module with mainboard

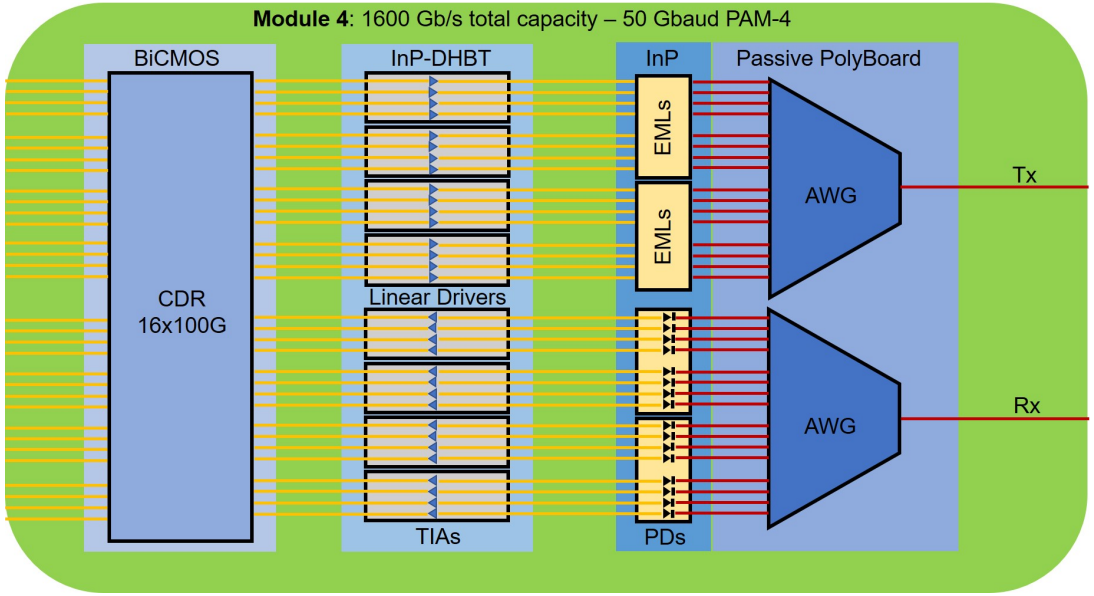


Module 1: 400 Gb/s pluggable

Module 2: 800 Gb/s mid-board

Module 3: 800 Gb/s pluggable

Module 4: 1.6 Tb/s mid-board



Roles and responsibilities of partners

- System design and definition of integration and packaging engine
- Development of components and integration engine for Terabit optical subassemblies
- Development of InP-DHBT linear driver arrays and selection of BiCMOS electronics
- Packaging of TERIPHIC modules
- System integration, testing and performance evaluation
- Exploitation, roadmaps and manufacturability studies

Contact

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